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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,349	12/11/2001	Gennaidy Poberezhskiy	ST00027USU (129-US-U1)	1645
27498 7590 08/24/2009 PILLSBURY WINTHROP SHAW PITTMAN LLP P.O. BOX 10500 MCLEAN, VA 22102			EXAMINER RAMAKRISHNAIAH, MELUR	
			ART UNIT 2614	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/020,349	Applicant(s) POBEREZHSKIY ET AL.	
	Examiner Melur Ramakrishnaiah	Art Unit 2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 June 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 recites among other things: "a sampling block coupled to the local oscillator, for receiving a discrete, non-continuous reference signal and the sampling clock and for generating reference sample signals". Applicant does not disclose this in his specification. In fact the specification discloses just the opposite of what is recited above as shown here. Page 7 of applicant's specification discloses the following: The sampling block 102 of the present invention performs sampling and quantization of the **incoming harmonic signal 106** whose frequency ... various devices can be used as a sampling block 102, ranging dedicated analog-to-digital converter (ADC) to a regular IC input pin (page 7 lines 4-9). As can be seen from this sampling block 102 receives incoming harmonic signal 106 which is a continuous signal, and not a discrete, non-continuous signal as claimed by the applicant in claim 1.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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4. Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 recites among other things: a sampling block coupled to the local oscillator, for receiving a discrete, non-continuous reference signal and the sampling clock and for generating reference sample signals". But applicant's specification discloses: The sampling block 102 of the present invention performs sampling and quantization of the incoming harmonic signal 106 (page 7 lines 4-5). If the sampling block 102 is receiving a discrete, non-continuous signal as claimed in claim 1. what is the need for sampling and quantization of this signal which is already a discrete, non-continuous reference signal.

Therefore current rejection is maintained as will be explained below.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-4, 5, are rejected under 35 U.S.C. 103(a) as being unpatentable over Morinaga et al. (JP07-106920, hereinafter Morinaga) in view of Patrick et al. (US PAT: 6,928,275, filed 5-8-2000, hereinafter Patrick).

Regarding claim 1, Morinaga discloses an apparatus for estimating frequency errors in locally generated clock signal for receivers, comprising: a local oscillator (5, Drawing 6) for generating a clock signal and a sampling clock, a sampling block (reads

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on 7/8, Drawing 6) coupled to the local oscillator, for receiving a discrete, non-continuous reference signal and the sampling clock and for generating reference sample signals, and a local oscillator frequency error estimator (11, Drawing 1), for generating an error estimate between the reference signal and local oscillator sampling clock (paragraph: 0042).

Regarding claim 5, Morinaga discloses a method of calibrating a local oscillator in a mobile receiver, comprising: receiving discrete, non-continuous reference signal from a source (7/8, Drawing 6) providing the reference signal, sampling the reference signal and the clock signal from the local oscillator (5, Drawing 6)) and providing a second reference signal, and estimating the error in the local oscillator using the second reference signal (paragraph: 0042).

Morinaga differs from claims 1, 5 in that he does not explicitly disclose GPS receiver for processing signals.

However, Patrick discloses method and apparatus for compensating local oscillator frequency error in GPS receiver for processing signals as shown in fig. 4 (col. 7, line 36 - col. 8, line 19).

Thus, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify Morinaga's system to provide for the following: GPS receiver for processing signals as this arrangement would provide means to receive and process GPS signals as thought by Patrick

Regarding claim 2, Morinaga further teaches the following: error estimate approximates a frequency difference between the reference signal and the clock signal (Paragraph: 0042).

Regarding claim 3, Morinaga teaches the following: sampling block comprises a block selected from a group comprising dedicated analog-to-digital converter and integrated (IC) input pin (reads on 7/8, Drawing 6)

Regarding claim 4, Morinaga teaches the following: oscillator frequency estimator is selected from a group comprising a discrete Fourier transform, a frequency detector, and a phase detector (paragraph: 0046)

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morinaga in view of Patrick as applied to claim 5 above, and further in view of Evans et al. (US PAT: 6,240,556, hereinafter Evans).

Regarding claim 6, the combination does not teach the following: sampling and estimating are performed by software instructions to a microprocessor.

However, Evans discloses subscriber frequency control system which teaches the following: sampling and estimating are performed by software instructions to a microprocessor (see abstract and col. 4 lines 50-57).

Thus, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify the combination to provide for the following: sampling and estimating are performed by software instructions to a microprocessor as this arrangement would provide another well known method of implementing frequency error estimation as taught by Evans.

Response to Arguments

8. Applicant's arguments filed on 6-3-09 have been fully considered but they are not persuasive.

Rejection of claims 1-6 under 35 U.S.C 103(a) as being obvious over Morinaga et al. (JP07-106920, hereinafter Morinaga) in view of Patrick et al. (US PAT: 6,928,275, filed 5-8-2000, hereinafter Patrick): Applicant argues that "Morinaga does not teach or discloses a sampling block receiving a discrete, non-continuous reference signal of claim 1 for the following reasons. First in Drawing 6 of Morinaga, there is no sampling block 102 (fig. 1) coupled to a local oscillator that receives a "discrete, non-continuous reference signal" and generates reference sample signals". Regarding this, Applicant's disclosure does not support this claim limitation. In fact applicant's specification discloses: The sampling block 102 of the present invention performs sampling and quantization of the incoming harmonic reference signal 106 (page 7 lines 4-5). As can be seen from this, sampling block 102 is receiving an harmonic signal, which is not a discrete, non-continuous signal as claimed by the applicant, which is subject to sampling and quantization. So Morinaga's drawing 6 shows sampling block (reads on A/D converter) which does sampling to do the quantization based on sampling frequency to produce discrete signal which is similar to what applicant's specification discloses as explained above. The combination Morinaga in view of Patrick does what applicant has disclosed in the specification and therefore rejection of claims 1-6 is maintained as set forth above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melur Ramakrishnaiah whose telephone number is (571)272-8098. The examiner can normally be reached on 9 Hr schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curt Kuntz can be reached on (571) 272-7499. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Melur Ramakrishnaiah/
Primary Examiner, Art Unit 2614